

*A' Sub B' →*  
*END*  
wherein the semiconductor element is secured with such a stress level applied on a back thereof that when the semiconductor element is detached from the board, the semiconductor element at least partially deforms due to the stress.

*Sub B2 →*  
4. (Amended) The semiconductor device as defined in claim 1, wherein the semiconductor element has a thickness of 50  $\mu$ m or less in the area where the semiconductor element is secured.

*A2 cont*  
*Sub D1 →*  
5. (Amended) The semiconductor device as defined in claim 1, wherein the semiconductor element is specified to include a transistor section wherein transistors are provided at high density, the transistor section at least partially deforming convexly or concavely due to the stress when detached from the board.

6. (Amended) The semiconductor device as defined in claim 1, wherein the semiconductor element includes detector means for detecting an electrical property developing only when the semiconductor element is level, so as to control operation of the integrated circuit.

*need the transistor associated w/ page*

*Sub B3 →*  
7. (Amended) A method of manufacturing a semiconductor device, comprising,

securing a semiconductor element having an integrated circuit to a board so as to be level with the board,

securing at least a part of a back of the semiconductor element to the board so as to develop a stress level that reacts when the semiconductor element is detached from the board, causing

Sub B3  
at least a part of the semiconductor element to deform, wherein the semiconductor element operates normally only when the semiconductor device is level.

8. (Amended) The method of manufacturing a semiconductor device as defined in claim 7,

AD  
End  
wherein the securing at least a part of a back step is specified to be carried out by at least one technique selected from a group consisting of scraping by means of dicing, sand blast, and sandpaper and treatment by means of laser beam projection.

9. (Amended) The method of manufacturing a semiconductor device as defined in claim 7,

wherein the securing step results in the semiconductor element having a thickness of 50  $\mu$ m or less where the semiconductor element is secured.

**Please add the following new claims 21-22:**

Sub D  
21  
Cont  
--21. (New) A semiconductor device, in which a semiconductor element with an integrated circuit is secured to a board,

wherein the semiconductor element is secured in a level position and specified to operate normally only when the semiconductor element is maintained in this level position,

wherein the semiconductor element includes detector means for detecting an electrical property developing within the semiconductor element only when the semiconductor element is level, so as to control operation of the integrated circuit.

A

22. (New) A method of manufacturing a semiconductor device,  
comprising,

securing a semiconductor element having an integrated  
circuit to a board so as to be level with the board,

securing at least a part of a back of the semiconductor  
element to the board so as to develop a stress level that reacts  
when the semiconductor element is detached from the board, causing  
at least a part of the semiconductor element to deform

wherein the securing at least a part of a back is  
specified to be carried out by at least one technique selected from  
a group consisting of scraping by means of dicing, sand blast, and  
sandpaper and treatment by means of laser beam projection.